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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,662	07/17/2003	Karsten Wieczorek	2000.104200	2057

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,662	WIECZOREK ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/621662.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al (US 6,455,362) in view of IBM Technical Disclosure Bulletin, December 1984, Vol 27, Issue 7B

Tran discloses a method for improving DRAM refresh. The method comprises the steps of:

providing a substrate having partially formed thereon semiconductor devices, the devices comprising first and second sidewall spacers of oxide and nitride (col 7, lines 23-25), which reads on providing a substrate havjng partially formed thereon semiconductor devices, the devices comprising first and second sidewall spacers with first and second etch rates with respect to a specific etchant, whereby the first etch rate

is lower than the second etch rate since it is known in the art that oxide and nitride have different etch rate with respect to a specific etchant, whereby one etch rate is lower than the other (see prior art of record for evidence of this basis)

implanting ions into the first sidewall spacer (col 7, lines 65-67; fig. 5)

removing the first and second sidewall spacers with the specific etchant (col 8, lines 43-50)

Unlike the instant claimed inventions as per claims 1, 8-9, Tran fails to specifically disclose implanting inert ions into the sidewall spacer to adapt the first etch rate to the second etch rate/increase the selectivity in removing the first and second sidewall spacers

IBM Technical Bulletin, December 1984, discloses a method for improve source/drain diffusion comprises the step of implanting inert/argon ions into the oxide sidewall spacer (page 4362; fig. 4) to increase the etch rate of the sidewall spacer/increase the selectivity in removing the sidewall spacer

Thus, one skilled in the art at the time the invention was made would have found it obvious to modify Tran method by implanting inert/argon ions into the sidewall spacer to increase/adapt the etch rate/increase the selectivity in removing the first and second sidewall spacers as per IBM Technical Bulletin because the IBM Technical Bulletin discloses that the argon implantation is designed to penetrate the oxide spacer, allowing the oxide to be etched at much faster rate

Regarding claims 2-3, Tran discloses partially formed semiconductor devices are partially formed N-type and P-type field effect transistor in a MOS structure (col 8, lines 1-5)

Regarding claims 4-7, Tran discloses forming a mask covering the second sidewall spacer when implanting the ions into the first spacers (col 7, lines 31-33; fig. 6)

The limitations of claims 8-9, 13-15 have been discussed above

Regarding claims 10-11, Tran discloses that the implanting dose is $1x\ 10^{15}$ atoms/ions/cm^2 at an energy level of 30-100 keV (col 7, lines 64-65; col 8, lines 23-25)

Regarding claim 12, Tran discloses implanting at an angle between 0-45 degrees (col 7, lines 51-52)

Regarding claims 16-17, Tran discloses the step of implanting with boron (col 8, lines 25-29)

Regarding claim 18, Tran discloses that the thickness of layer 72/gate feature is 30 angstroms<100 nm (col 10, lines 19-20)

3. Claims 19-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al (US 6,455,362) in view of IBM Technical Disclosure Bulletin, December 1984, Vol 27, Issue 7B

Tran discloses a method for improving DRAM refresh. The method comprises the steps of:

providing a substrate having partially formed thereon semiconductor devices, the

devices comprising first and second sidewall spacers of oxide and nitride (col 7, lines 23-25), which reads on providing a substrate havjng partially formed thereon semiconductor devices, the devices comprising first and second sidewall spacers with first and second etch rates with respect to a specific etchant, whereby the first etch rate is lower than the second etch rate since it is known in the art that oxide and nitride have different etch rate with respect to a specific etchant, whereby one etch rate is lower than the other (see prior art of record for evidence of this basis)

implanting ions into the first sidewall spacer (col 7, lines 65-67; fig. 5)

removing the first and second sidewall spacers with the specific etchant (col 8, lines 43-50)

Unlike the instant claimed inventions as per claims 19, 22-23, Tran fails to specifically disclose implanting inert ions into the sidewall spacer to increase the first etch rate and second etch rate/increase the selectivity in removing the first and second sidewall spacers

IBM Technical Bulletin, December 1984, discloses a method for improve source/drain diffusion comprises the step of implanting inert/argon ions into a spacer (page 4362; fig. 4) to increase the etch rate of the sidewall spacer/increase the selectivity in removing the sidewall spacer

Thus, one skilled in the art at the time the invention was made would have found it obvious to modify Tran method by implanting inert/argon ions into the sidewall spacer to increase the etch rates/increase the selectivity in removing the first and second sidewall spacers as per IBM Technical Bulletin because the IBM Technical Bulletin discloses that

the argon implantation is designed to penetrate the spacer material, allowing the spacer to be etched at much faster rate

Regarding claims 20-21, Tran discloses partially formed semiconductor devices are partially formed N-type and P-type field effect transistor in a MOS structure (col 8, lines 1-5)

The limitations of claims 22-23, 27-29 have been discussed above

Regarding claims 24-25, Tran discloses that the implanting dose is $1x\ 10^{15}$ atoms/ions/cm^2 at an energy level of 30-100 keV (col 7, lines 64-65; col 8, lines 23-25)

Regarding claim 26, Tran discloses implanting at an angle between 0-45 degrees (col 7, lines 51-52)

Regarding claims 30-31, Tran discloses the step of implanting with boron (col 8, lines 25-29)

Regarding claim 32, Tran discloses that the thickness of layer 72/gate feature is 30 angstroms<100 nm (col 10, lines 19-20)

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chang et al (US 6,346,449) discloses that oxide and nitride have different etch rate/etch selectivity with respect to a specific etchant, whereby one etch rate is lower than the other (col 5, lines 1-7)

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
April 27, 2005